WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

(a) a P-channel transistor composed of a first group of sections;

(b) an N-channel transistor composed of a second group of sections; and

(c) the sections of the first group being alternately located with respect to the sections of the second group so as to form a generally checkerboard pattern in a first interdigitated output stage area of the integrated circuit including the P-channel transistor and the N-channel transistor wherein a higher amount of heat normally generated in the N-channel transistor is dissipated over the entire interdigitated output stage area to reduce peak temperatures in the N-channel transistor.

2. The integrated circuit of claim 1 including a fully differential amplifier including a first differential input stage including a first interdigitated output stage including the P-channel transistor and the N-channel transistor, and also including a second differential input stage including a second interdigitated output stage substantially similar to the first interdigitated output stage.

3. An integrated circuit comprising:

(a) a P-channel transistor composed of a first group of sections, each section of the first group including a source region, a drain region, and a gate;

(b) a plurality of N-type well regions in which the sections of the first group are respectively disposed, the source regions in the first group all being electrically connected together, the drain regions in the first group all being electrically connected together, and the gates in the first group all being electrically connected together;

(c) an N-channel transistor composed of a second group of sections, each section of the second group including a source region, a drain region, and a gate;

(d) a plurality of P-type well regions in which the sections of the second group are respectively disposed, the source regions in the second group all being electrically connected together, the drain regions in the second group all being electrically connected together, and the gates in the second group all being electrically connected together; and

(e) the sections of the first group being alternately located with respect to the sections of the second group so as to form a generally checkerboard pattern in an interdigitated output stage area of the integrated circuit including the P-channel transistor and the N-channel transistor wherein a higher amount of heat normally generated in the N-channel transistor is

dissipated over the entire interdigitated output stage area to reduce peak temperatures in the N-channel transistor.

4. The integrated circuit of claim 3 including a fully differential amplifier including a first differential input stage including a first interdigitated output stage including the P-channel transistor and the N-channel transistor, and also including a second differential input stage including a second interdigitated output stage substantially similar to the first interdigitated output stage.

5. The integrated circuit of claim 3 wherein the sections of the first group and the sections of the second group are arranged in a generally checkerboard pattern.

6. The integrated circuit of claim 5 wherein the sections of the first group and the sections of the second group are disposed in a generally rectangular surface area of the integrated circuit including a complementary output stage that includes the P-channel transistor and the N-channel transistor.

7. The integrated circuit of claim 5 wherein the sections of the first group and the sections of the second group are disposed in a generally rectangular surface area of integrated circuit including an H-bridge circuit, wherein the P-channel transistor and the N-channel transistor are transistors that are simultaneously in an on condition during normal operation of the H-bridge circuit.

8. The integrated circuit of claim 3 wherein the safe current-conducting capabilities of the P-channel transistor and the N-channel transistor are approximately equal.

9. The integrated circuit of claim 5 including a temperature-sensing transistor of a thermal shut-down circuit located within a hot spot region in which the highest temperatures would be most likely to occur during operation of the integrated circuit.

10. The integrated circuit of claim 9 wherein the temperature-sensing transistor is part of a shut-down circuit included in the integrated circuit and configured to turn off the P-channel transistor and the N-channel transistor for at least a predetermined amount of time if the temperature within the hot spot region increases to a predetermined level that activates the shut-down circuit.

11. The integrated circuit of claim 10 wherein the predetermined level is greater than approximately 150 degrees centigrade.

12. The integrated circuit of claim 3 wherein the number of sections of the first group is equal to the number of sections of the second group.

13. The integrated circuit of claim 3 where the sections of the first group and the sections of the second group are generally rectangular.

14. The integrated circuit of claim 3 wherein the generally checkerboard pattern in the interdigitated output stage area is generally square.

15. The integrated circuit of claim 3 including a plurality of P-type moat regions surrounding the plurality of N-type well regions, respectively, and a plurality of N-type moat regions surrounding the plurality of P-type well regions, respectively.

16. The integrated circuit of claim 4 wherein the first differential input stage includes a first input coupled to receive a first input signal, a second input coupled by a first conductor to a first terminal of a first resistor and to a first terminal of a second resistor, and an output coupled to a second terminal of the first resistor, and wherein the second differential input stage includes a first input coupled to receive a second input signal, a second input coupled by a second conductor to a first terminal of a third resistor and to a second terminal of the second resistor, and an output coupled to a second terminal of the third resistor.

17. A method of reducing peak hot spot temperatures in an integrated circuit comprising:

(a) segmenting a P-channel transistor into a first group of sections;

(b) segmenting an N-channel transistor into a second group of sections; and

(c) alternately locating the sections of the first group with respect to the sections of the second group so as to form a generally checkerboard pattern in an interdigitated output stage area of the integrated circuit including the P-channel transistor and the N-channel transistor wherein a higher amount of heat normally generated in the N-channel transistor is dissipated over the entire interdigitated output stage area to reduce peak temperatures in the N-channel transistor.

18. The method of claim 17 including arranging the sections of the first group and the sections of the second group in a generally checkerboard pattern.

19. The method of claim 18 including arranging the sections of the first group and the sections of the second group in a generally rectangular surface area of the integrated circuit including a complementary output stage that includes the P-channel transistor and the N-channel transistor.

20. The method of claim 19 including arranging the sections of the first group and the sections of the second group in a generally rectangular surface area of integrated circuit including an H-bridge circuit, wherein the P-channel transistor and the N-channel transistor are transistors that are simultaneously in an on condition during normal operation of the H-bridge circuit.

21. The method of claim 20 including configuring the P-channel transistor and the N-channel transistor so that there safe current-carrying capabilities are approximately equal.

22. The method of claim 17 including providing a temperature-sensing transistor of a thermal shut-down circuit located within a hot spot region in which the approximately the highest temperatures would be most likely to occur during operation of the integrated circuit.

23. The method of claim 22 including operating a thermal shut-down circuit to turn off the P-channel transistor and the N-channel transistor for at least a predetermined amount of time if the temperature within the hot spot region increases to a predetermined level that activates the shut-down circuit.

24. The method of claim 23 wherein the predetermined level is greater than approximately 150 degrees centigrade.

25. The method of claim 17 including providing an equal number of sections of the first and second groups.

26. An integrated circuit comprising:

(a) means for segmenting a P-channel transistor into a first group of sections;

(b) means for segmenting an N-channel transistor into a second group of sections; and

(c) means for alternately locating the sections of the first group with respect to the sections of the second group so as to form a generally checkerboard pattern in an interdigitated output stage area of the integrated circuit including the P-channel transistor and the N-channel transistor wherein a higher amount of heat normally generated in the N-channel transistor is dissipated over the entire interdigitated output stage area to reduce peak temperatures in the N-channel transistor.

27. The integrated circuit of claim 26 including temperature-sensing means of a thermal shut-down circuit located within a hot spot region in which the approximately the highest temperatures would be most likely to occur during operation of the integrated circuit.

28. The integrated circuit of claim 27 wherein the temperature-sensing means is part of a shut-down circuit included in the integrated circuit and configured to turn off the P-channel transistor and the N-channel transistor for at least a predetermined amount of time if the temperature within the hot spot region increases to a predetermined level that activates the shut-down circuit.

29. A method of reducing harmonic distortion in an integrated circuit comprising:

(a) segmenting a P-channel transistor into a first group of sections;

(b) segmenting an N-channel transistor into a second group of sections; and

(c) alternately locating the sections of the first group with respect to the sections of the second group so as to form a generally checkerboard pattern in an interdigitated output stage area of the integrated circuit including the P-channel transistor and the N-channel transistor wherein heat generated in the N-channel transistor and the P-channel transistor is dissipated over the entire interdigitated output stage area so as to reduce peak temperatures and so as to produce a uniform temperature profile across the integrated circuit.